

D1 43. (TWICE AMENDED) The circuit according to claim ~~13~~ 3

[12], wherein said [programmable] logic block [circuit] comprises a product term array.

D2 34. (THREE TIMES AMENDED) The circuit according to

claim ~~12~~, wherein said programmable logic circuit comprises [a look-up table] one or more logic blocks.

D3 7. (FOUR TIMES AMENDED) The circuit according to claim

~~12~~, wherein said reference clock [frequency] is selected from two or more reference clock signals [frequencies] in response to [(i) a multiplexer and (ii)] a configuration signal.

D3 8. (FOUR TIMES AMENDED) The circuit according to claim 7, wherein said two or more reference clock signals [frequencies] are generated internally to said device.

9. (FOUR TIMES AMENDED) The circuit according to claim 7, wherein said two or more reference clock signals [frequencies] are generated externally to said device.

D4 10. (THREE TIMES AMENDED) The device according to claim

~~12~~, wherein said programmable logic circuit comprises a [A] device selected from a group consisting of programmable logic devices

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(PLDs), complex programmable logic devices (CPLDs) and field programmable gate arrays (FPGAs) [, comprising the device of claim 12].

1 12. (THREE TIMES AMENDED) A device comprising:

a programmable logic circuit configured to (i) generate one or more control signals and (ii) receive one or more clock signals; and

5 a phase lock loop circuit configured to generate said one or more clock signals, each capable of oscillating at a different one of a plurality of frequencies, said clock signals generated in response to (i) a reference clock, [and] (ii) said one or more control signals, and (iii) one or more of said clock signals 10 wherein said programmable logic circuit and said phase lock loop circuit are integrated on a single circuit.

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12. (THREE TIMES AMENDED) A method for [providing an integrated] dynamically changing a frequency of operation of a programmable logic circuit [and a phase lock loop circuit] comprising the steps of:

(a) [manipulating information] configuring said programmable logic circuit to generate one or more control signals and receive one or more clock signals; and

(i) capable of oscillating at a different one of a plurality of frequencies, and

(ii) generated in response to a reference clock, one or more of said clock signals, [frequency] and said one or more control signals.

15 more control signals.

12 1619. (THREE TIMES AMENDED) The method according to claim  
15, further comprising the step of:

more external clock signals generated externally to said  
5 programmable logic circuit.

5 programmable logic circuit.

*13* 18. further comprising the step of:

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18. further comprising the step of:

5 said programmable logic circuit.

means for implementing programmable logic for manipulating information to generate one or more control signals.

wherein said means for implementing programmable logic receives one  
5 or more clock signals; and

means for generating said one or more clock signals in  
response to (i) a reference clock, [and] (ii) said one or more  
control signals, and (iii) one or more of said clock signals  
wherein said one or more clock signals are each capable of  
oscillating at a different one of a plurality of frequencies, said  
means for implementing programmable logic and said means for  
generating are integrated on a single circuit.

#### SUPPORT FOR CLAIM AMENDMENTS

Support for the amendments to the claims may be found in  
the drawings (e.g., FIGS. 1 and 2) and the specification (e.g.,  
page 6, lines 15-22), as originally filed. As such, no new matter  
has been added.

#### R E M A R K S

Careful review and examination of the subject application  
are noted and appreciated.

The present invention concerns a device comprising a  
programmable logic circuit and a phase lock loop circuit. The  
programmable logic circuit may be configured to (i) generate one or  
more control signals and (ii) receive one or more clock signals.

The phase lock loop circuit may be configured to generate the one